CLAIMS

1. A data processing system, comprising:

a first bus master;

a second bus master; and

a shared reconfigurable resource accessible by the first bus master and the second bus master, wherein the shared reconfigurable resource establishes a communication path between at least one of the first and second bus masters and circuitry for performing a first peripheral function selected from a plurality of peripheral functions.

2. The data processing system of claim 1, wherein the shared reconfigurable resource comprises reconfigurable channel circuitry which comprises at least a portion of the circuitry for performing the first peripheral function.

3. The data processing system of claim 2, wherein the shared reconfigurable resource comprises reconfigurable channel storage accessible by the reconfigurable channel circuitry for use in performing the first peripheral function.

4. The data processing system of claim 2, wherein the reconfigurable channel circuitry is configurable to perform a second peripheral function selected from the plurality of peripheral functions.

5. The data processing system of claim 4, wherein the shared reconfigurable resource establishes a second communication path between at least one of the first and second bus masters and circuitry for performing the second peripheral function, and wherein the reconfigurable channel circuitry comprises at least a portion of the circuitry for performing the second peripheral function.

6. The data processing system of claim 5, wherein the circuitry for performing the second peripheral function comprises at least one of a serial peripheral interface (SPI), a universal asynchronous receiver/transmitter (UART), a universal serial bus (USB), an input capture, an output compare, a general purpose input/output, a timer, and a synchronous serial interface (SSI).

7. The data processing system of claim 1, wherein the data processing system further comprises first peripheral function circuitry coupled to the shared reconfigurable resource, wherein the first peripheral function circuitry comprises at least a first portion of the circuitry for performing the first peripheral function.

8. The data processing system of claim 7, wherein the shared reconfigurable resource comprises at least a second portion of the circuitry for performing the first peripheral function.

9. The data processing system of claim 8, wherein the shared reconfigurable resource establishes a second communication path between at least one of

the first and second bus masters and circuitry for performing a second peripheral function selected from the plurality of peripheral functions.

10. The data processing system of claim 9, wherein the data processing system further comprises second peripheral function circuitry coupled to the shared reconfigurable resource, wherein the second peripheral function circuitry comprises at least a first portion of the circuitry for performing the second peripheral function and the shared reconfigurable resource comprises at least a second portion of the circuitry for performing the second peripheral function.

11. The data processing system of claim 8, wherein the circuitry for performing the second peripheral function comprises at least one of a serial peripheral interface (SPI), a universal asynchronous receiver/transmitter (UART), a universal serial bus (USB), an input capture, an output compare, a general purpose input/output, a timer, and a synchronous serial interface (SSI).

12. The data processing system of claim 1, wherein the circuitry for performing the first peripheral function comprises at least one of a serial peripheral interface (SPI), a universal asynchronous receiver/transmitter (UART), a universal serial bus (USB), an input capture, an output compare, a general purpose input/output, a timer, and a synchronous serial interface (SSI).

13. A method for operating a reconfigurable resource, comprising:

configuring the reconfigurable resource to establish a first communication path between a first master and circuitry for performing a first peripheral function; and

configuring the reconfigurable resource to establish a second communication path between a second master and circuitry for performing a second peripheral function, each of the first and second peripheral functions selected from a plurality of peripheral functions.

14. The method of claim 13 wherein configuring the reconfigurable resource to establish the first communication path comprises configuring channel circuitry within the reconfigurable resource to perform the first peripheral function.

15. The method of claim 14, wherein configuring the reconfigurable resource to establish the second communication path comprises configuring the channel circuitry within the reconfigurable resource to perform the second peripheral function.

16. The method of claim 15, wherein the first bus master and the second bus master are different masters coupled to the reconfigurable resource.

17. The method of claim 15, wherein the first bus master and the second bus master are a same master coupled to the reconfigurable resource.

18. The method of claim 15, wherein configuring the channel circuitry to perform the first peripheral function and configuring the channel circuitry

to perform the second peripheral function each comprises configuring channel storage coupled to the channel circuitry.

19. The method of claim 15, wherein the first peripheral function and the second peripheral function comprise a same peripheral function.

20. The method of claim 15, wherein the first peripheral function and the second peripheral function comprise different peripheral functions.

21. The method of claim 13, wherein the plurality of peripheral functions comprise at least one of a serial peripheral interface (SPI) function, a universal asynchronous receiver/transmitter (UART) function, a universal serial bus (USB) function, an input capture function, an output compare function, a general purpose input/output function, a timer function, and a synchronous serial interface (SSI) function.

22. A shared reconfigurable resource, comprising:

reconfigurable channel storage configurable to store information associated with a plurality of peripheral functions;

reconfigurable channel circuitry, configurable to perform each of the plurality of peripheral functions; and

control logic, coupled to the reconfigurable channel storage and the reconfigurable channel circuitry, wherein the control logic configures the reconfigurable channel storage and reconfigurable channel circuitry to perform a selected one of the plurality of peripheral functions.

23. The shared reconfigurable resource of claim 22, wherein the control logic establishes a communication path between at least one of a plurality of masters and circuitry for performing the selected one of the plurality of peripheral functions.

24. The shared reconfigurable resource of claim 23, wherein the reconfigurable channel circuitry comprises at least a portion of the circuitry for performing the selected one of the plurality of peripheral functions.

25. The shared reconfigurable resource of claim 22, wherein the control logic indicates to the reconfigurable channel storage and the reconfigurable channel circuitry the selected one of the plurality of peripheral functions.

26. The shared reconfigurable resource of claim 22, wherein the plurality of peripheral functions comprises a first of a serial peripheral interface (SPI) function, a universal asynchronous receiver/transmitter (UART) function, a universal serial bus (USB) function, an input capture function, an output compare function, a general purpose input/output function, a timer function, and a synchronous serial interface (SSI) function.

27. The shared reconfigurable resource of claim 26, wherein the plurality of peripheral functions comprises a second of a serial peripheral interface (SPI) function, a universal asynchronous receiver/transmitter (UART) function, a universal serial bus (USB) function, an input capture function,

an output compare function, a general purpose input/output function, a timer function, and a synchronous serial interface (SSI) function.

28. The shared reconfigurable resource of claim 22, wherein a first subset of the plurality of peripheral functions correspond to a first master and a second subset of the plurality of peripheral functions correspond to a second master.

29. A shared Universal Serial Bus (USB) resource comprising:

a bus interface which communicates with a first master and a second master;

endpoint storage circuitry, coupled to the bus interface, the endpoint storage circuitry comprising a plurality of endpoints wherein each of the plurality of endpoints is allocatable to one of the first master and the second master;

a serial interface engine which communicates with a USB host; and

a USB function controller, coupled to the bus interface, endpoint storage circuitry, and serial interface engine, the USB function controller comprising:

USB protocol logic, coupled to the serial interface engine;

endpoint interrupt logic which generates interrupts based on information received from the USB protocol logic;

interrupt steering registers; and

interrupt steering logic which routes each of the interrupts to a corresponding one of the first master and the bus master based

on steering information provided by the interrupt steering registers.

30. The shared USB resource of claim 29, wherein the plurality of endpoints are allocated based on the interrupt steering registers.

31. The shared USB resource of claim 30, wherein, for each of the plurality of endpoints, the interrupt steering registers indicate allocation to one of the first master and the second master.

32. The shared USB resource of claim 30, wherein the interrupt steering registers comprise an interrupt steering set register and an interrupt steering clear register.

33. The shared USB resource of claim 32, wherein the interrupt steering registers further comprise interrupt steering storage circuitry coupled to the interrupt steering set register and the interrupt steering clear register, the interrupt steering storage circuitry providing the steering information to the interrupt steering logic.

34. The shared USB resource of claim 33, wherein the interrupt steering storage circuitry comprises a plurality of set-reset latches.

35. A shared Universal Serial Bus (USB) resource comprising:

a plurality of endpoints wherein each of the plurality of endpoints is allocatable to one of a plurality of bus masters;

a USB function controller, coupled to the plurality of endpoints, the USB function controller comprising:

endpoint interrupt logic which generates interrupts based on communication from a USB host;

at least one interrupt steering register accessible by the plurality of bus masters; and

interrupt steering logic which routes each of the interrupts to a corresponding bus master of the plurality of bus masters based on steering information provided by the interrupt steering registers.

36. The shared USB resource of claim 35, wherein the at least one interrupt steering register comprises an interrupt steering set register and an interrupt steering clear register.

37. The shared USB resource of claim 36, wherein the at least one interrupt steering registers further comprise interrupt steering storage circuitry coupled to the interrupt steering set register and the interrupt steering clear register, the interrupt steering storage circuitry providing the steering information to the interrupt steering logic.